Appl. No.: 09/343,872
Amdt. dated May 5, 2004
Reply to Office action of March 17, 2004

AMENDMENT

Amendment to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (Currently amended) A data transfer apparatus that comprises:

~~a plurality of~~ a first group of bus lines~~ses each~~ configured to ~~couple~~ transfer data bits between a first processing device ~~to~~and a corresponding first memory module;

a second group of bus lines configured to transfer data bits between a second processing device and a corresponding second memory module;

~~at least one~~a group of cross-bus lines configured to transfer data bits between the first group of bus lines and the second group of bus lines via bus bridges ~~coupled to each of the plurality of busses by one or more bus bridges, wherein the bus bridges each include a set of multiplexers that are configurable to steer signals from the bus to the cross-bus, and are further configurable to steer signals from the cross-bus to the bus~~; and

a memory management unit configured to receive memory access requests from ~~a plurality of~~the first and second processing devices and to responsively configure the bus bridges to steer address and data signals accordingly,

wherein ~~the plurality~~each group of bus lines~~ses~~ includes two unidirectional bit lines for each data bit ~~and the at least one cross-bus includes two unidirectional bit line for each data bit~~, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines.

2. (Currently amended) The data transfer apparatus of claim 1, wherein the memory management unit includes a DMA controller coupled to the group of cross-bus lines and configurable to transfer a block of data between said memory modules.

3. (Original) The data transfer apparatus of claim 2, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to said processing devices after completing a block transfer of data.

4. (Original) The data transfer apparatus of claim 1, wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word transfers.

5. (Original) The data transfer apparatus of claim 4, wherein said one or more request queues includes a block transfer queue configured to store access requests relating to block data transfers.

6. (Original) The data transfer apparatus of claim 4, wherein said one or more request queues includes a message transfer queue configured to store message transfer requests.

7. (Original) The data transfer apparatus of claim 6, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request.

8. (Currently amended) The data transfer apparatus of claim 1, further comprising:
port logic connected to the first and second groups~~plurality~~ of bus~~ses~~ lines and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory.

9. (Canceled)

10. (Currently amended) The data transfer apparatus of claim 1, wherein each group~~said plurality~~ of bus~~ses~~ lines includes at least three ~~busses~~unidirectional bit lines.

11. (Previously presented) A method for transferring data between a set of memory modules and a set of processor units, wherein the method comprises:

said processing units providing transfer requests to a memory manager;

said memory manager setting a router in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes:

said memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses,

wherein the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit,

wherein the bus bridges each include a multiplexer for each outgoing bit line that selects from multiple incoming bit lines; and

said processing units accessing memory modules via said router.

12. (Original) The method of claim 11, wherein before setting said router, said memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request.

13. (Original) The method of claim 11, wherein said setting said router further includes:

said memory manager operating a direct memory access (DMA) controller to perform block transfers of data between memory modules.

14. (Original) The method of claim 11, further comprising said memory manager asserting an interrupt signal to any one of said processor units that is the addressee of a message transfer request.

15. (Currently amended) A high-bandwidth bus which comprises:

a plurality of local ~~busses~~ line groups each for transferring data between a processing device and an associated memory module;

~~a~~ cross-bus lines for transferring data among the plurality of local ~~busses~~ line groups, wherein said cross-bus is coupled to each of the plurality of local ~~busses~~ line groups by a bridge means that includes bi-directional data channel bridges and uni-directional address channel bridges; and

a memory controller means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules

wherein the local ~~busses~~ line groups each include ~~two~~oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes ~~two~~oppositely configured unidirectional bit lines for each data bit.

16. (Currently amended) A high-bandwidth bus system which comprises:

a plurality of local memory busses each for transferring data between a processing device and an associated memory module;

one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection and wherein the local intersect busses are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses; and

a memory controller means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules

wherein the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each includes two unidirectional bit lines for each data bit.

17. (Previously presented) The bus system of claim 16, wherein the four multiplexers forward data between a processing device and a memory device with essentially no latency delay.

18. (Previously presented) The bus system of claim 17, further comprising a memory management unit that includes a DMA controller coupled to the local intersect busses and configurable to transfer a block of data between said memory modules.

19. (Previously presented) The bus system of claim 18, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to said processing devices after completing a block transfer of data.

20. (Previously presented) The bus system of claim 18, wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word transfers.

21. (Previously presented) The bus system of claim 20, wherein said one or more request queues includes a block transfer queue configured to store access requests relating to block data transfers.

22. (Previously presented) The bus system of claim 20, wherein said one or more request queues includes a message transfer queue configured to store message transfer requests.

23. (Previously presented) The bus system of claim 22, wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request.

24. (Previously presented) The bus system of claim 18, further comprising:
port logic connected to the plurality of local memory busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory.

25. (New) A system, comprising:
a plurality of processors;
a plurality of memory modules, each memory module being coupled to and paired with one of the processors via separate sets of bus lines such that a data read requested from processor to a paired memory module is received on a first clock cycle subsequent to a clock cycle that provides an address;
a set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable between the sets of bus lines via the cross-bus lines,
wherein the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable.

26. (New) The system of claim 25 wherein at least two sets of the bus lines have different widths.